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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,616	12/19/2000	Lizy Kurian John	UTAU:1100RCE	5809

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CHALKER FLORES, LLP
2711 LBJ FRWY
Suite 1036
DALLAS, TX 75234

EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,616	JOHN ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-29 and 31-38* is/are rejected.

7)☒ Claim(s) *11 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/08/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-38 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,2,8-10,13-19, 20,21, 23-27, 31, 35-37 , 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. (5,651,123) in view of Sourgen et al. (5,781,470).

3. As to claim 1, 20,31, 38, the "processor" (claim1, and 38) is read as any type of processing system. Applicant is welcome to give feedback in the next response.

4. Nakagawa disclosed a system including at least :

a) a sequence generator that generate one or more resource identifiers (ID) using at least portion of the pseudo sequence within a processor (e.g. see col.8, lines 38-67, col.9, lines 1-1 1 , see also fig.8 for the corresponding index 07-00);
b) resource identifier selector (selector) coupled to the sequence generator (e.g. see (figs.3,5,15 see also col.7, lines 26-67, col.8, lines 1-5) for selecting one or more resource id for instruction allocation.

5. Nakagawa taught a generation of resource identifiers corresponding to a processor resource (memory location) (e.g. .see col.7, lines 25-29). Nakagawa

generated program was directed to addresses corresponding to locations in an instruction memory. The locations in the instruction memory are processor resources because instructions are being used by the processor.

c) selectors for selecting an identifier (address of an instruction) in , col.7, lines 25-29) from one or more identifiers (see a series of random numbers by the selectors in See also Nakagawa's fig.3 , random generator, which included plurality of col.7, lines 33-58) allocated to the instruction (i.e. outputting of instruction address for a given instruction).

6. Nakagawa also included at least :.

a) memory storage device (e.g. see fig.4 (Memory));

b) a bus (fig.4 (364);

c) a processor (30) coupled to the bus comprising a resource allocator (see fig.4).

7. As to the determination of how many resource identifiers are required by the decoded instruction as newly claimed, Nakagawa also determined how many id's needed (e.g. see the number sequence of 0-126 in col.8, lines 1-12).

8. Nakagawa did not specifically show his pseudorandom resource identifiers allocation to the decoded instruction as claimed. However, Sourgen disclosed a system including a decoded write instruction and a generated pseudorandom value allocated for the decoded write instruction (see how the microprocessor decoded the write instruction , and generated the pseudo random value to activate the write pulse in col.6,

lines 1-9, see the purpose of pseudorandom generator for write pulse in col.5, lines 58-62). It would have been obvious to one of ordinary skill in the art to use Sourgen in Nakagawa for allocating the pseudorandom resource identifiers to the decoded instruction as claimed because the use of Sourgen could provide Nakagawa the ability to assign the resource identifiers (e.g. Nakagawa's pseudorandom generated addresses) into a predefined level of processing, e.g. the decode stage, thereby reducing the waiting cycle for decoding whenever the instruction was ready for execution, and because Nakagawa also taught his pseudo random resource identifiers were generated based on a selection signal applied by a decoder which decoded a read instruction (see col.5, lines 11-16), and one of ordinary skill in the art should be able to recognize that the resource identifiers could be applicable to the decoded instruction as the resource identifiers might have been the destinations address specified in the instruction already decoded, and for above, reasons , provided a suggestion.

9. As to the selection of resource identifiers for allocation to the decoded instruction (see claim 1, last two lines), applicant argued that Nakagawa 's random number counter (e.g. the resource identifiers) works with instruction decoder prior to the decoding by the decoder 34. See reasons of obviousness set forth in paragraph above.

10. As to claim 2, Nakagawa also determined how many id's needed (e.g. see the number sequence of 126 in col.8, lines 1-12).

11. As to claims 8-10, Nakagawa disclosed logic circuit (fig.5 (selection) and storage array (see fig.5 Register).

12. As to claim 12, Nakagawa was also directed to pseudorandom sequence (e.g. see col.3, lines 35-36).

13. As to claim 13, Nakagawa also generated a pseudorandom number based on a first pseudo number (e.g. see the sequential generation of he random numbers in fig.8).

14. As to claims 14, 17, 23,35-37, Nakagawa also stored the random number as elements in a storage array (e.g. see each value of the random number in respective register in fig.5, see also the selector for the logic circuit and the register array for the storage array).

15. As to claims 15, 18,24, Nakagawa also included least significant bit (e.g. see fig.8 00 bit in the table).

16. As to claims 16,25, Nakagawa also included a shifter (e.g. see the feedback shift register in col.4, lines 13-24) and the selection circuit for indexing the element of the array (e.g. see the selection of the output address in col.7, lines 25-67, col.8, lines 1-5).

17. As to claim 19, Nakagawa also determined the highest identifier (e.g. see the 1-126 range in col.8, lines 1-12).

18. As to claim 21, Nakagawa also determined how many identifiers required (e.g. see, col.2, lines 29-41 , col.8, lines 1-8).

19. As to claim 26, Nakagawa also included determining a number based the most recent associated identifier (e.g. see the fixed sequence of the random numbers in col.1-6).

20. As to claim 27, Nakagawa's identifier was also associated with instruction (e.g. see col.9, lines 12-22, see the random number of each instruction in figs.8-12).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 3 ,4 are rejected under 35 U.S.C. 103(a) as being unpatentable over

22. Nakagawa et al. (5,651 ,123) in view of Sourgen et al. (5,781,470) as applied to claim 1 above, and further in view of Gupta et al. (5,490,280)

23. As to claims 3,4, Neither Nakagawa nor Sourgen disclosed the reorder buffer the buffer entries and as claimed. However, Gupta disclosed a reorder buffer and buffer entries (e.g. see fig.,1B, fig.2). It would have been obvious to one of ordinary skill in the art to use Gupta in Nakagawa for including the reorder buffer and the buffer entries as

claimed because the use of Gupta could provide the control capability of Nakagawa to easily allocate the resource information (e.g. id, data etc.) in a predetermined , thereby providing operand data requested at specific order of the instruction execution sequence from a single set of buffer entries, and therefore, reducing the latency cycle caused by separate hardware circuit, and it could be readily done by predefining the reorder buffer of Gupta into Nakagawa with modified configuration parameters (e.g. the buffer RM port), such that the reorder buffer of Gupta could be recognized by Nakagawa, and one of ordinary skill in the ad should be able to recognize that the locking mechanism of Nakagawa's arbitration among the plurality of peripheral devices would have needed a storage buffer, such as reorder buffer , for providing specific operation order of the resources to enhance the arbitration, and in doing so, provided a motivation.

24. Claims 5,6,7,22,28, 29, 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. (5,651,123) in view of Sourgen et al. (5,781,470) as applied to claims 1, 20,31 above, and further in view of Williams et al. (5,530,837).

25. As to claims 5,6,7,22, 28,29, 32-34, limitations of the parent clams have been discussed in the previous paragraph, therefore, they are not repeated herein. Nakagawa did not specifically show his selector comprised the comparator for comparing the ID to an allocation bound as claimed. However, Williams discloses system for including a comparison of allocation bound (range) (see the bank id and the range comparison (e.g. see col.5, lines 56-65, col.6, lines 6-22). It would have been

obvious to one of ordinary skill in the ad to use Williams in Nakagawa for including the comparator for comparing the resource id with the allocation bound as claimed because the use of Williams could provide Nakagawa the processing ability to allocate the id into a predetermined range of the resource identification , and therefore, eliminating possible contentions of the resource assignment by providing the comparison of he given range, and because it would have been obvious to one or ordinary skill in the ad to recognize that allocation of the resource id within a defined group of allocation range or bound seemed to be logical and desirable in order to minimize the conflicts among the resource id's, otherwise, the system could not worked in efficient manner, and for the above reasons provided motivation .

26. Claims 11,30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teach the combined features of the generation of the decoder stall signal by the resource identifiers selector issued to the instruction decoder whenever the one or more resource identifiers are not allocatable to the decoded instruction (claim 11), the comparison and the associating of the selected resource identifiers and the decode stall signal in response to the determination the resource within the processor corresponding to the selected resource identifier is not allocatable (claim 30).

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Togawa (6,038,585) is cited for the teaching of an instruction resource id (see the instruction book ID in col.5, lines 1-67);

b) Lafauci (6,507,808) is cited for the teaching of pseudorandom number for instruction operand (see col.5, lines 50-67).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP